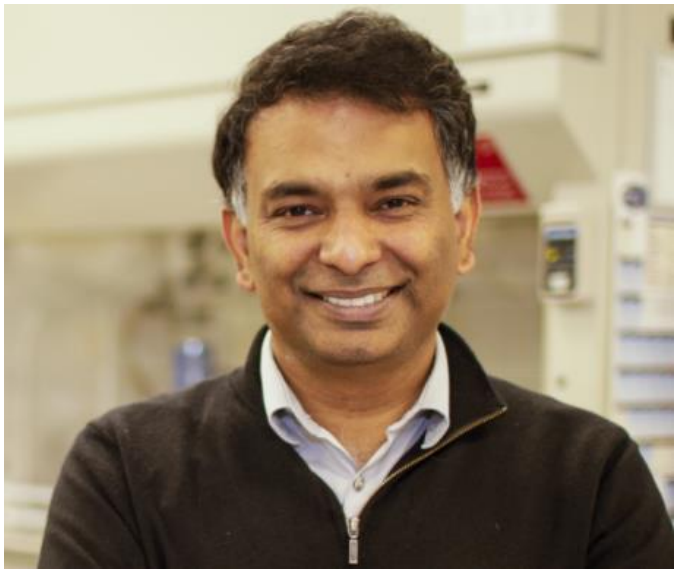
Seminar: **Development and R2R Scale up of a Hybrid Printed CMOS Silicon TFT Process**

Presenter: **Arvind Kamath, Vice President, Technology Development at Thin Film Electronics, Inc.**

Location: Microelectronics and Engineering Research Center (MER 160), Room 2.114, 10100 Burnet Road, Austin TX 78758

Time: Friday, Dec 08, 2017, at 2:00 - 3:30 PM CDT. *Pizza will be provided.*

Abstract: Low cost disposable wireless electronics that power the Internet of Everything (IoE) is an emerging class of devices. These provide everyday labels and packaging with Near Field Communication (NFC) standards based RF communication and adequate sensor based "intelligence. Very low cost at ultra large volumes is essential. A Printed Dopant Poly-Silicon (PDPS) silicon thin film transistor (TFT) CMOS technology, fabricated on a thin stainless steel substrate has been developed for this purpose. The talk will focus on the key technology features and challenges of taking this from concept to high volume roll to roll production. Roadmap work with flex-hybrid assembly of 3 bit sensor labels will be briefly described.



Arvind Kamath received a B.Tech degree in Metallurgical Engineering from the Indian Institute of Technology, Chennai and a Ph.D in Materials Science and Engineering from The University of Texas at Austin in 1997. From 1997 to 2004 he worked at LSI Logic in managerial and individual contributor roles. From 2004 to 2013, he worked at Kovio Inc. leading technology development and integration. He is currently Vice President, Technology Development at Thin Film Electronics, leading process technology R&D, roll to roll scale up and sensor development.