**Seminar:** **Is VLSI scaling dead? (Should you have picked computer science as a major?)**

**Presenter:** **Dr. Greg Yeric, Research Fellow, ARM Holdings**

**Location:** Microelectronics and Engineering Research Center (MER 160), Room 2.114, 10100 Burnet Road, Austin TX 78758

**Time**: Friday, May 12, 2017, at 3:30 PM CDT.

**Abstract**: What's going on with Moore's Law? Everyone has an opinion, and everyone's is different. You're about to get one more. Summary: It's complicated, but you're OK with your current major. Dr. Yeric will try to touch on the big ticket items in the industry: FinFETs, EUV, nanowires, copper wires, etc., and will happily attempt to take your questions about anything along those lines.

**Greg Yeric** earned his BSEE, MSEE, and PhD in Microelectronics at The University of Texas at Austin, in 1987, 1989, and 1993, respectively. That's correct: 10 years straight, living in the Engineering Science Building. Somehow, he maintained his sanity and has even outlived the building. His longest-lasting career achievement so far has been getting the MRC's original cleanroom up and running (later it was moved from ENS to MERB). He fought many battles with some of the Spin Rinse Dryers, at right, (you thought Samsung washing machines were dangerous?) the Karl Suss aligner, below, and the Blue M oven (he has a secret pencil eraser trick for that one). Most of his Master's degree learning centered on polypropylene and PVC welding for wet hoods. Also, all of the furnace endcap carriers, like the one you see at lower right. All are personally hand-crafted by Greg, including the stands. If you bring one to the talk, he will autograph it for you.

After UT, Greg started at Motorola's Advanced Products Research and Development Laboratories in the area of semiconductor process integration, subsequently working at TestChip Technologies, HPL Technologies, and Synopsys, in the areas of test structures, technology development, and yield analysis. For the last 9 years, he has been with ARM Holdings in Austin, Texas, where he is a Research Fellow in the area of future silicon technology. His group's activities include novel technology, design-technology co-optimization and predictive technology modeling.

(Abstract and Biography Provided by Speaker)